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Minimization of Power Dissipation In VLSI Systems Using Hardware Description Languages

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ABSTRACT: *The need for low power and high efficiency electronics is felt more and more with the proliferation of complex mobile gadgets into our daily use. This paper describes about implementation of low power techniques using hardware description languages (VERILOG HDL) through simulation and synthesis. The power reports after synthesis indicate that there is considerable amount of power saving when these low power techniques are applied.*

Keywords: *Low Power, VLSI Circuits, Simulation, Synthesis, HDL, Verilog.*

I. INTRODUCTION

In all the battery operated devices, there is a need to reduce power dissipation to avoid frequent recharging and thereby increase battery life, reduce the size of battery, and cooling system needed for removing the heat. So it is necessary to reduce the power dissipation in IC's. Power Dissipation can be minimized at various levels like System level, Behavioral level, Architectural level, Circuit level, Physical design, and Technology level. There is considerable effort put in, throughout the world, to reduce power dissipation in VLSI circuits, to increase the life of the battery and to prevent hot spots. There are several approaches suggested [1-9]. Chandrakasan etal.[1] have described about techniques for Low-Power CMOS Digital Design. Bipul C. Paul etal.[9] have described about Low power design techniques for scaled technologies. This paper, describes about application of various low power techniques using Verilog hardware description language through simulation and synthesis. The various low power techniques are given below.

II. LOW POWER TECHNIQUES

One-hot and Gray encoding consume lesser power as compared to binary encoding because one-hot and gray encodings have only a single bit change while going from one state to another as shown below so that number of transitions are reduced i.e. switching activity is reduced so that power is reduced.

Decimal value	Binary code	Gray code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

For example a counter with binary state machine encoding goes from state3 to state 4 i.e. from 0011 to 0100 then the number of transitions are three whereas for gray code state machine encoding from state3 to state4 i.e.

0010 to 0110 only one transition will take place. Thus, by using the gray counter we can reduce the switching activity and thereby reduce the power dissipation in the designs. Gray encoding consumes lesser power as compared to binary encoding. Any logic element will contribute to power consumption as it has a capacitance attached to it and transitioning of data through that logic will lead to power dissipation.

The RTL coding should be carried out in a manner that there are no unwanted or redundant logic elements. Any logic element will contribute to power consumption as it has a capacitance attached to it and transitioning of data through that logic element will lead to power dissipation. Resource sharing is an optimization technique that uses a single functional block (such as an adder or comparator) to implement several operators in the HDL code.

Register timing is a concept mostly used in improving timing by reordering the combinational and sequential logic in a given data path. In certain cases, there is a saving of logic and thus can help improve upon power consumption.

Certain operations require more computational energy than others. In DSP circuits, multiplication and addition are the two most important operations performed. Multiplication consumes more energy per computation than addition. Hence, replacing multiplication by addition can save power so that energy per consumption is reduced. This is achieved at the cost of small increase in delay. Reducing the operation count leads to reduction of total capacitance associated with the system and hence can reduce power dissipation.

In many instances, data is loaded into register infrequently, but the clock signal continues to switch at every clock cycle which drives a large capacitive load. Sometimes registers are assigned the same value for every clock cycle. To prevent clock from triggering the registers, a gating circuit can be used to shut off the clock from these circuits.

In the traditional synchronous designs style used for most HDL and synthesis-based designs, the system clock is connected to the clock pin on every flip-flop in the design. This results in two major components of power consumption: power consumed by combinatorial logic whose values are changing on each clock edge, power consumed by flip-flops (this has a non-zero value even if there is no input to the flip-flop). These two types of power consumed can be saved by deactivating clock signal when there are no transitions on the input.

i. SIMULATION AND SYNTHESIS RESULTS OF DESIGNS

Some of the simulation and synthesis results of the designs when the low power techniques are applied are shown below. The functionality of the designs has been verified through simulation by using NC-Verilog tool. The net lists and power reports after synthesis have been generated by using the RTL compiler tool of CADENCE.

The Simulation waveforms with binary encoding are shown in Figure1. In this figure, clk, reset, count are the single bit inputs and currentstate is the 16 bit output. During posedge of rst, current state will be in s0 state i.e 0000 irrespective of the input count. Now if count=1'b1 then output starts counting. As this is a binary counter, it counts 0001, 0010 and so on for each positive clock edge.

The Simulation waveforms of 16 bit counter with gray coding are shown in Figure2. In this figure, clk, reset, count are the single bit inputs and currentstate is the 16 bit output. During positive edge of rst, current state will be in s0 state i.e 0000 irrespective of the input count. Now if rst is low and count=1'b1 then output starts counting. As this a gray counter it counts 0001,0003,0002,0006 and so on for each positive clock edge. Here transitions are reduced on currentstate output compared to output of binary counter shown in Figure1.

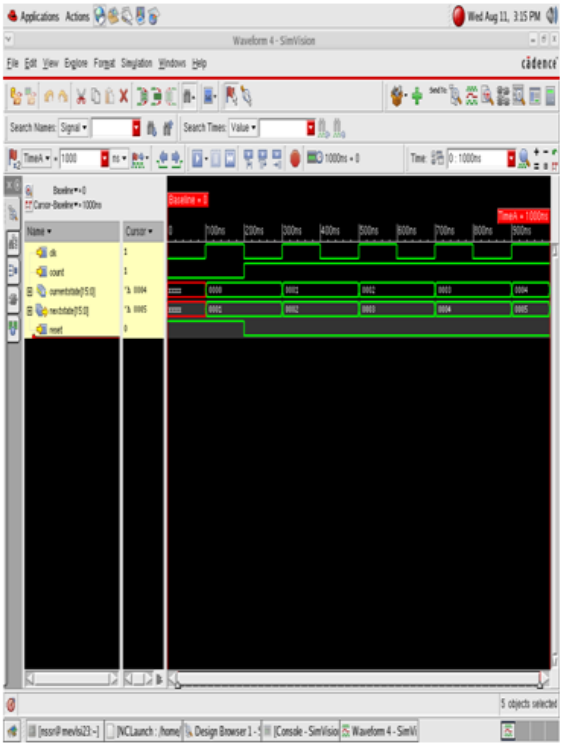

Figure1: Simulation waveforms of 16 bit counter using binary encoding

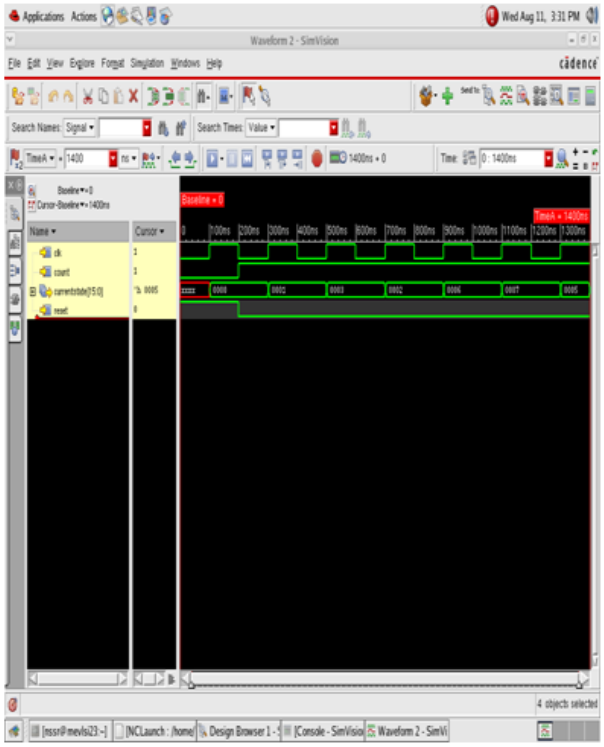

Figure2: Simulation waveforms of 16 bit counter using gray code encoding

The Simulation waveforms without the application of operation reduction are shown in Figure3. In this figure a, b, x are the 16 bit inputs and p, q, r are the 16 bit intermediate wires and y is the 16 bit output. The whole implementation is $y=x^2 + ax + b$ so that p is assigned x*x, q is assigned a*x and r is assigned b. For example a=16'h0007, b=16'h0009, x=16'h0006 then p=16'h0024 (i.e. decimal 36), q=16'h002A, r=16'h004E finally z=p + q + r=16'h0057. The Simulation waveforms with operation reduction are shown in Figure4 which gives same results.

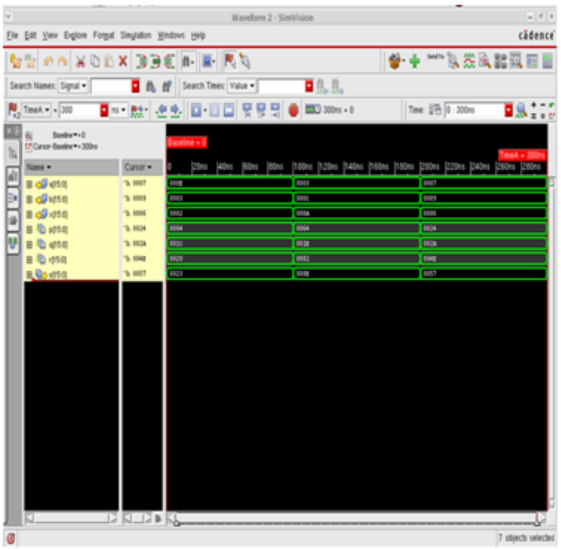

Figure3: Simulation waveforms without the application of operation reduction.

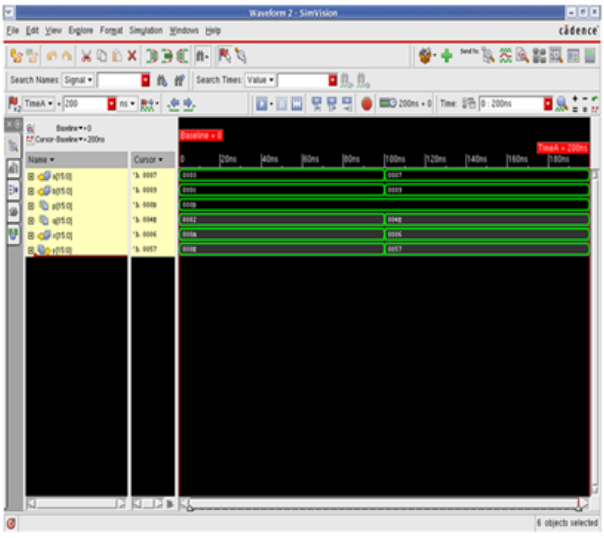

Figure4: Simulation waveforms with the application of operation reduction.

III. CONCLUSION

This paper reports about power reduction in VLSI circuits using low power techniques for different types of designs through simulation and synthesis. The design styles mentioned in this paper have a significant impact on the overall power consumption of the circuits and they do not affect the functionality of the designs.

Low power technique	**Power dissipation without low power technique**	**Power dissipation with low power technique**
Gray code in place of binary code	204812 nW	186981 nW
Resource sharing	45776 nW	34433 nW
Register retiming	839154 nW	440651 nW
Operation substitution	271402 nW	131864 nW
Operation reduction	274084 nW	269955 nW
Clock Gating	506543 nW	339822 nW

Table1. Power dissipation in designs with and without application of low power techniques.

REFERENCES

[1] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low-Power CMOS Digital Design", IEEE Journal of Solid-state Circuits, Vol. 27, pp. 473-483, 1992.

[2] Rung-Bin Lin and Chi-Ming Tsai, "Theoretical Analysis of Bus-Invert Coding", IEEE Transactions on Very Large Scale Integration(VLSI systems), Vol. 10, NO. 6, December 2002.

[3] Diary Rawoof Sulaiman, "Using Clock gating Technique for Energy Reduction in Portable Computers", IEEE Proceedings of the International Conference on Computer and Communication Engineering 2008.

[4] Walter Aloisi and Rosario Mita, "Gated-Clock Design of Linear-Feedback Shift Registers", IEEE Transactions on circuits and systems—II: Express Briefs, Vol. 55, NO. 6, JUNE 2008.

[5] Xin Wang, Peter Noel and Tad Kwasniewski, "low power design techniques for a montgomery modular multiplier", Proceedings of 2005 International Symposium on Intelligent Signal Processing and Communication Systems, December 13-15 2005.

[6] D. Liu and C. Svensson, "Power consumption estimation in CMOS VLSI chips," IEEE Journal of Solid State Circuits, Vol. 29, NO.6, pp.663-670, 1994.

[7] L. Benini and G. De Micheli, "State Assignment for Low-Power Dissipation," Proc. IEEE Custom Integrated Circuits Conf, Piscataway, N.J., 1994, pp.137-139.

[8] E. Macii, R. Mehra,M. Poncino, "Micro-Architectural Power Estimation and Optimization," Chapter 13 of: EDA for IC System Design, Verification, and Testing, 2006 Taylor & Francis Group.

[9] Bipul C . paul, amit Agarwal and Kaushik Roy, "Low power design techniques for scaled technologies", INTEGRATION, the VLSI Journal, Vol. 39, issue 2, 2006, pp. 64-89.